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## TECHNOLOGIES

[CCD vs. CMOS](#)



## CCD vs. CMOS

The technologies and the markets that use them continue to mature, but the comparison is still a lot like apples vs. oranges: they can both be good for you. DALSA offers both.

CCD (charge coupled device) and CMOS (complementary metal oxide semiconductor) image sensors are two different technologies for capturing images digitally. Each has unique strengths and weaknesses giving advantages in different applications. Neither is categorically superior to the other, although vendors selling only one technology have usually claimed otherwise. In the last five years much has changed with both technologies, and many projections regarding the demise or ascendance of either have been proved false. The current situation and outlook for both technologies is vibrant, but a new framework exists for considering the relative strengths and opportunities of CCD and CMOS imagers.

Both types of imagers convert light into electric charge and process it into electronic signals. In a **CCD** sensor, every pixel's charge is transferred through a very limited number of output nodes (often just one) to be converted to voltage, buffered, and sent off-chip as an analog signal. All of the pixel can be devoted to light capture, and the output's uniformity (a key factor in image quality) is high. In a **CMOS** sensor, each pixel has its own charge-to-voltage conversion, and the sensor often also includes amplifiers, noise-correction, and digitization circuits, so that the chip outputs digital bits. These other functions increase the design complexity and reduce the area available for light capture. With each pixel doing its own conversion, uniformity is lower. But the chip can be built to require less off-chip circuitry for basic operation. For more details on device architecture and operation, see our original "[CCD vs. CMOS: Facts and Fiction](#)" article and its 2005 update, "[CMOS vs. CCD: Maturing Technologies, Maturing Markets](#)."

CCDs and CMOS imagers were both invented in the late 1960s and 1970s (DALSA founder and CEO Dr. Savvas Chamberlain was a pioneer in developing both technologies). CCD became dominant, primarily because they gave far superior images with the fabrication technology available. CMOS image sensors required more uniformity and smaller features than silicon wafer foundries could deliver at the time. Not until the 1990s did lithography develop to the point that designers could begin making a case for CMOS imagers again. Renewed interest in CMOS was based on expectations of lowered power consumption, camera-on-a-chip integration, and lowered fabrication costs from the reuse of mainstream logic and memory device fabrication. While all of these benefits are possible in theory, achieving them in practice while simultaneously delivering high image quality has taken far more time, money, and process adaptation than original projections suggested (see "[CMOS Development's Winding Path](#)" below).

Both CCDs and CMOS imagers can offer excellent imaging performance when designed properly. CCDs have traditionally provided the performance benchmarks in the photographic, scientific, and industrial applications that demand the highest image quality (as measured in quantum efficiency and noise) at the expense of system size. CMOS imagers offer more integration (more functions on the chip), lower power dissipation (at the chip level), and the possibility of smaller system size, but they have often required tradeoffs between image quality and device cost. Today

## DALSA PRODUCTS



[CCD and CMOS sensors](#)



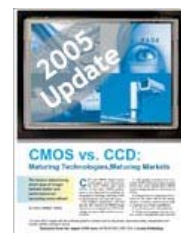
[CCD and CMOS cameras:](#)

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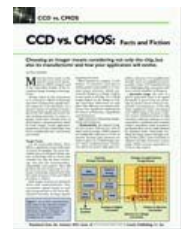
## MORE INFORMATION



[Applications Set Imager Choices](#) by Nixon O, in Advanced Imaging, July 2008 (PDF)



**2005 Update:**  
[CMOS vs. CCD: Maturing Technologies, Maturing Markets](#) by Dave Litwiller, in Photonics Spectra August 2005 (421k PDF)



[CCD vs. CMOS: Facts and Fiction](#) by

there is no clear line dividing the types of applications each can serve. CMOS designers have devoted intense effort to achieving high image quality, while CCD designers have lowered their power requirements and pixel sizes. As a result, you can find CCDs in low-cost low-power cellphone cameras and CMOS sensors in high-performance professional and industrial cameras, directly contradicting the early stereotypes. It is worth noting that the producers succeeding with "crossovers" have almost always been established players with years of deep experience in both technologies.

Costs are similar at the chip level. Early CMOS proponents claimed CMOS imagers would be much cheaper because they could be produced on the same high-volume wafer processing lines as mainstream logic or memory chips. This has not been the case. The accommodations required for good imaging performance have required CMOS designers to iteratively develop specialized, optimized, lower-volume mixed-signal fabrication processes--very much like those used for CCDs. Proving out these processes at successively smaller lithography nodes (0.35um, 0.25um, 0.18um...) has been slow and expensive; those with a captive foundry have an advantage because they can better maintain the attention of the process engineers.

CMOS cameras may require fewer components and less power, but they still generally require companion chips to optimize image quality, increasing cost and reducing the advantage they gain from lower power consumption. CCD devices are less complex than CMOS, so they cost less to design. CCD fabrication processes also tend to be more mature and optimized; in general, it will cost less (in both design and fabrication) to yield a CCD than a CMOS imager for a specific high-performance application. However, wafer size can be a dominating influence on device cost; the larger the wafer, the more devices it can yield, and the lower the cost per device. 200mm is fairly common for third-party CMOS foundries while third-party CCD foundries tend to offer 150mm. Captive foundries use 150mm, 200mm, and 300mm production for both CCD and CMOS.

The larger issue around pricing is sustainability. Since many CMOS start-ups pursued high-volume, commodity applications from a small base of business, they priced below costs to win business. For some, the risk paid off and their volumes provided enough margin for viability. But others had to raise their prices, while still others went out of business entirely. High-risk startups can be interesting to venture capitalists, but imager customers require long-term stability and support.

While cost advantages have been difficult to realize and on-chip integration has been slow to arrive, speed is one area where CMOS imagers can demonstrate considerable strength because of the relative ease of parallel output structures. This gives them great potential in industrial applications.

CCDs and CMOS will remain complementary. The choice continues to depend on the application and the vendor more than the technology. DALSA's approach is "technology-neutral": we are one of the few vendors able to offer real solutions with both CCDs and CMOS.

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Dave Litwiller, in Photonics Spectra,  
January 2001 (385k PDF)

### Feature and Performance Comparison

Feature	CCD	CMOS
Signal out of pixel	Electron packet	Voltage
Signal out of chip	Voltage (analog)	Bits (digital)
Signal out of camera	Bits (digital)	Bits (digital)
Fill factor	High	Moderate
Amplifier mismatch	N/A	Moderate
System Noise	Low	Moderate
System Complexity	High	Low
Sensor Complexity	Low	High
Camera components	Sensor + multiple support chips + lens	Sensor + lens possible, but additional support chips common

Relative R&D cost	Lower	Higher
Relative system cost	Depends on Application	Depends on Application
Performance	CCD	CMOS
Responsivity	Moderate	Slightly better
Dynamic Range	High	Moderate
Uniformity	High	Low to Moderate
Uniform Shuttering	Fast, common	Poor
Uniformity	High	Low to Moderate
Speed	Moderate to High	Higher
Windowing	Limited	Extensive
Antiblooming	High to none	High
Biasing and Clocking	Multiple, higher voltage	Single, low-voltage

### CMOS Development's Winding Path

Initial Prediction for CMOS	Twist	Outcome
Equivalence to CCD in imaging performance	Required much greater process adaptation and deeper submicron lithography than initially thought	High performance available in CMOS, but with higher development cost than CCD
On-chip circuit integration	Longer development cycles, increased cost, tradeoffs with noise, flexibility during operation	Greater integration in CMOS, but companion chips still required for both CMOS and CCD
Reduced power consumption	Steady improvement in CCDs	Advantage for CMOS, but margin diminished
Reduced imaging subsystem size	Optics, companion chips and packaging are often the dominant factors in imaging subsystem size	CCDs and CMOS comparable
Economies of scale from using mainstream logic and memory foundries	Extensive process development and optimization required	CMOS imagers use legacy production lines with highly adapted processes akin to CCD fabrication